

Assouad, Patrick

From: Assouad, Patrick
Sent: Tuesday, June 21, 2005 7:32 AM
To: 'Pascale Hair'
Subject: RE: USSN 10/727,210 - Our Ref: PEA10US

Immediately below is what I currently see in the Image file:

App'n No. 10/727,210
 Amst. Dated April 26, 2005
 Response to Office Action of February 15, 2005

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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An integrated circuit, comprising a processor, an onboard system clock for generating a clock signal, and clock trim circuitry, the integrated circuit being configured to:
 - (a) receive an external signal;
 - (b) determine either the number of cycles of the clock signal during a predetermined number of cycles of the external signal, or the number cycles of the external signal during a predetermined number of the cycles of the external signal, or the number of cycles of the clock signal;
 - (c) output the result of the determination of step (b);
 - (d) receive a trim value from an external source;
 - (e)(e) store the trim value in the integrated circuit, the trim value having been determined on the basis of the determined number of cycles;
 - (f)(f) use the trim value to control the internal clock frequency.

Regards,
 Patrick Assouad

-----Original Message-----

From: Pascale Hair [mailto:pascale.hair@silverbrookresearch.com]
Sent: Tuesday, June 21, 2005 12:48 AM
To: Assouad, Patrick
Subject: USSN 10/727,210 - Our Ref: PEA10US

Dear Examiner Assouad,

I refer to the above US application.

It appears there are two versions of claim 1 and I would be grateful if you could confirm which is the current claim 1, **specifically, point (b)**, on file at the USPTO, that is:

Version 1:

1. An integrated circuit, comprising a processor, an onboard system clock for generating a clock signal, and clock trim circuitry, the integrated circuit being configured to:
 - (a) receive an external signal;
 - (b) determine either the number of cycles of the clock signal during a predetermined number of cycles of the external signal, or the number of cycles of the external signal during a predetermined number of cycles of the clock signal;**
 - (c) output the result of the determination of step (b);
 - (d) receive a trim value from an external source;
 - (e) store the trim value in the integrated circuit, the trim value having been determined on the basis of the determined number of cycles;
 - (f) use the trim value to control the internal clock frequency.

Version 2:

1. An integrated circuit, comprising a processor, an onboard system clock for generating a clock signal, and clock trim circuitry, the integrated circuit being configured to:
 - (a) receive an external signal;
 - (b) determine either the number of cycles of the clock signal during a predetermined number of cycles of the external signal, or the number cycles of the external signal during a predetermined number of the cycles of the external signal, or the number of cycles of the clock signal;**
 - (c) output the result of the determination of step (b);
 - (d) receive a trim value from an external source;
 - (e) store the trim value in the integrated circuit, the trim value having been determined on the basis of the determined number of cycles;
 - (f) use the trim value to control the internal clock frequency.

Part (b) of claim 1 was not amended during prosecution. Please kindly confirm which version you hold to enable us to respond appropriately to the Office Action dated June 6, 2005. Apologies for any inconvenience caused.

Yours sincerely,

Kia Silverbrook

Silverbrook Research Pty Ltd

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Peter C. [Signature]
6/21/05

(Authorization at
end of e-mail.)